Single Event Effects in FPGA Devices 2014-2015

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To be presented by Melanie Berg at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 23-26, 2015.

Acronyms

- Block random access memory (BRAM)
- Built-in-self-test (BIST)
- Combinatorial logic (CL)
- Commercial off the shelf (COTS)
- Complementary metal-oxide semiconductor (CMOS)
- Device under test (DUT)
- Digital Signal Processing Block (DSP)
- Distributed triple modular redundancy (DTMR)
- Edge-triggered flip-flops (DFFs)
- Field programmable gate array (FPGA)
- Global triple modular redundancy (GTMR)
- Joint test action group (JTAG)
- Input – output (I/O)
- Intellectual Property (IP)
- Internal configuration access port (ICAP)
- Linear energy transfer (LET)
- Local triple modular redundancy (LTMR)
- Look up table (LUT)
- Microprocessor (MP)
- Operational frequency (*fs)*
- *Processor (PC)*
- Phase locked loop (PLL)
- Power on reset (POR)
- Probability of flip-flop upset (P_{DFFSEU})
- Probability of logic masking (P_{logic})
- Probability of transient generation (P_{gen})
- Probability of transient propagation (P_{prop})
- Radiation Effects and Analysis Group (REAG)
- Single event functional interrupt (SEFI)
- Single event latch-up (SEL)
- Single event transient (SET)
- Single event upset (SEU)
- Single event upset cross-section (σ_{SEU})
- Static random access memory (SRAM)
- System on a chip (SOC)
- Transient width (τ_{width})
- Triple modular redundancy (TMR)
- Universal Serial Bus (USB)
- Windowed Shift Register (WSR)

Overview

- Review of FPGA Roadmap chart (previously presented by Kenneth LaBel).
- Work performed by NASA/GSFC:
  - Security and trust.
  - Radiation Testing:
    - Xilinx Virtex-5 (commercial) heavy ion testing,
    - Xilinx Kintex-7 heavy ion testing, and
    - Study of TMR mitigation techniques.
    - Radiation tests were performed with custom-built DUT boards that connect to the NEPP low cost digital tester (LCDT).
- Plans for FY15 and out:
  - Microsemi, Xilinx, Altera, Synopsis.

Review of FPGA Roadmap Chart: Field Programmable Gate Arrays (FPGAs)

Trusted FPGA

- ***DoD Development***

Altera

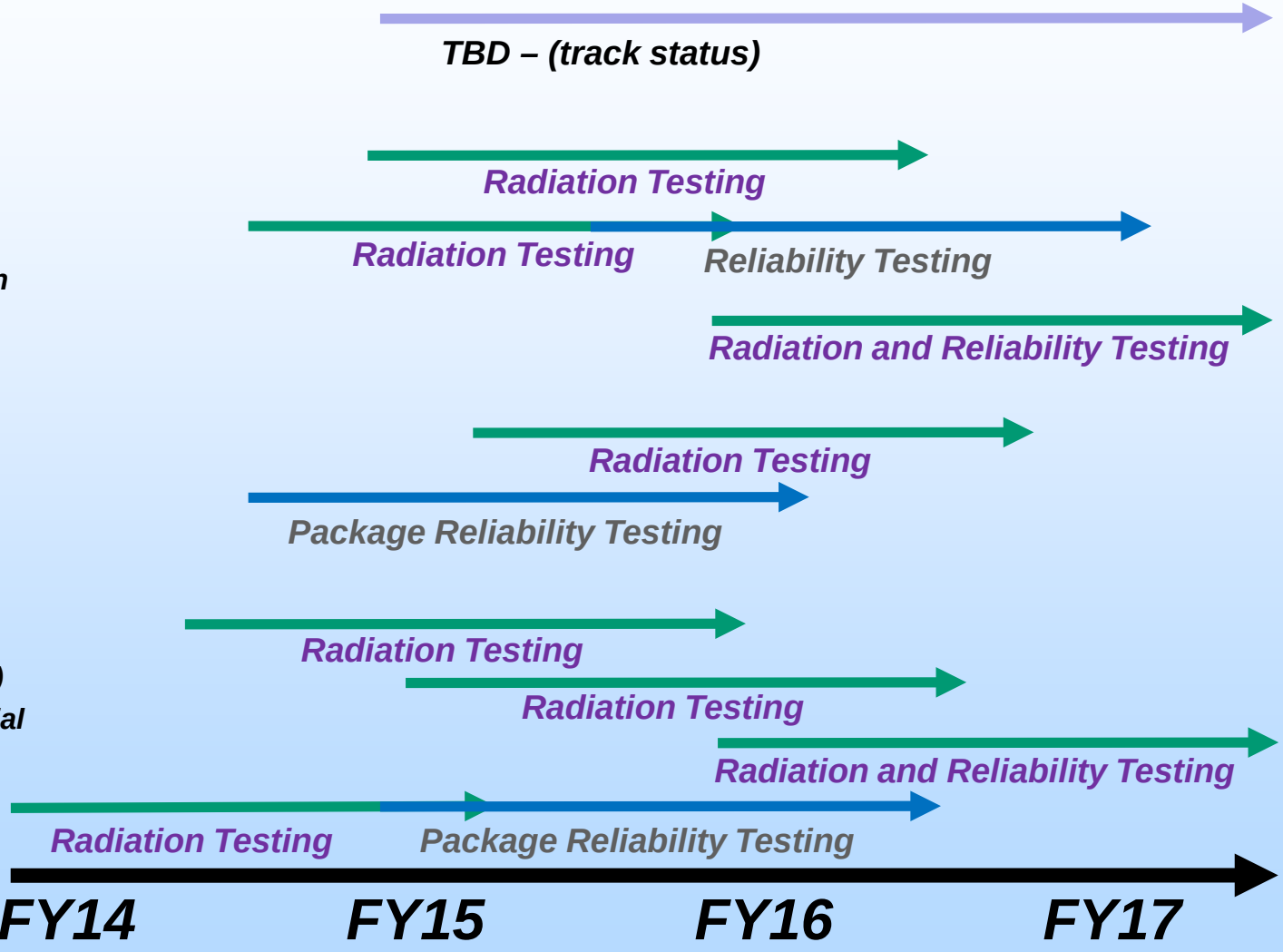
- ***Stratix 5 (28nm TSMC process commercial)***
- ***Max 10 (55nm NOR based commercial – small mission candidate)***
- ***Stratix 10 (14nm Intel process commercial)***

Microsemi

- ***RTG4 (65nm RH)***

Xilinx

- ***7 series (28nm commercial)***
- ***Ultrascale (20nm commercial – planar)***
- ***Ultrascale+ (16nm commercial - vertical)***
- ***Virtex 5QV (65nm RH)***



FY=Fiscal Year

FPGA Security and Trust

- **Goal: Support the U.S. government concerns over security and trust in FPGAs**
- **Conference participation:**
  - **Xilinx Security Working Group (XSWG) 2014 in Boulder/Longmont, CO.**
  - **Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2015 in St. Louis, MO.**
  - **Hardened Electronics and Radiation Technology (HEART) 2015 in Chantilly, VA.**
  - **Hardware-Oriented Security and Trust (HOST) 2015, McLean VA.**
- **Collaboration with Aerospace Corporation and other agencies.**

Xilinx Virtex-5 Heavy Ion SEU Testing
65nm bulk CMOS
XC5VFX130T

Xilinx Virtex-5 FPGA Investigation

- This was an independent study to determine the single event destructive and transient susceptibility of the Commercial Xilinx Virtex-5 device with special interest regarding its embedded PowerPC 440.
- A custom DUT board was designed to interface to the NEPP-LCDT. Maximizes DUT control and fault monitoring.
- The FPGA-DUT was configured to have various test structures that were geared to measure specific types of Single Event Effect (SEE) susceptibilities of the device.
- The DUT was monitored for single event transient (SET), single event upset (SEU), and single event latch-up (SEL) induced faults while exposing the devices to a heavy ion beam.
- Test strategies are based on the NEPP FPGA SEU-Test guidelines manual : https://nepp.nasa.gov/files/23779/fpga_radiation_test_guidelines_2012.pdf

Test Facility Conditions

- **Facility: Texas A&M University Cyclotron Single Event Effects Test Facility, 25 MeV/amu tune).**
- **Flux: 50-to-10000 particles/cm^{2}·s**
- **Fluence: All tests were run to 1 x 10^{7} particles/cm^{2} or until destructive or functional events occurred.**
- **Test temperature: Room temperature**

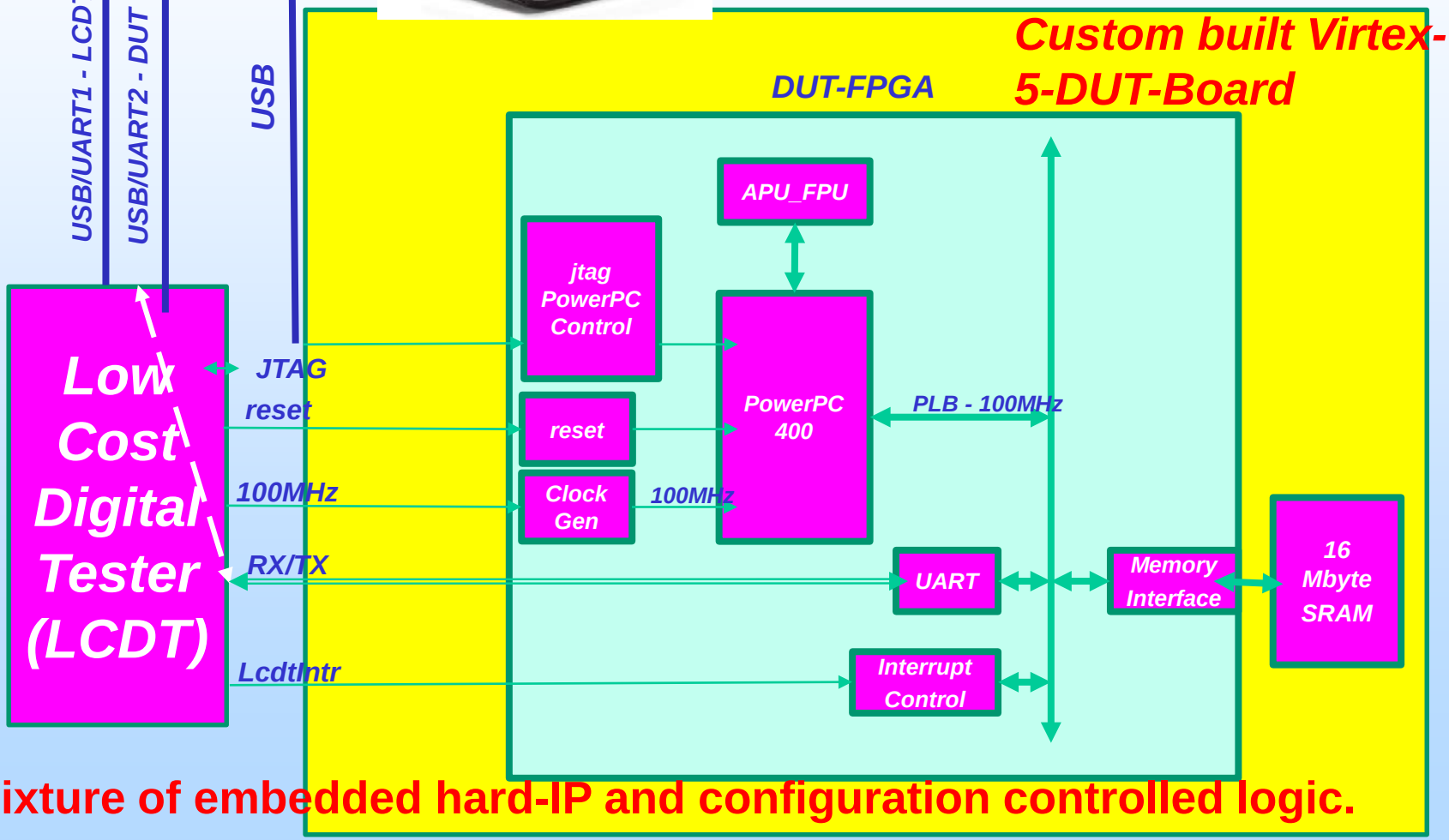
Ion	Energy (MEV/Nucleon)	LET (MeV*cm^{2}/mg) 0°	LET (MeV*cm^{2}/mg) 60 °
He	25	.07	.14
N	25	.9	.18
Ne	25	1.8	3.6
Ar	25	5.5	11.0
Kr	25	19.8	40.0
Xe	25	38.9	78.8

Test Run Conditions

- Total of 437 test runs were performed.
- Simple, slightly complex, up to complex test structures were selected for accelerated radiation testing.
- Simple test structures assist in data analysis because data can be extremely convoluted for complex test structures.
- Test structures utilized:
  - Configuration,
  - Windowed shift registers (WSRs),
  - Counters,
  - PLL,
  - BRAM+EDAC, and
  - PowerPC-440.
- Note: Some tests were run with the scrubber on versus the scrubber off in order to determine if scrubbing would affect the system SEU rate (non-mitigated system).

Block Diagram Test Environment for PowerPC 440

Arithmetic unit (APU); floating point unit (FPU);
Processor local bus (PLB);



Mixture of embedded hard-IP and configuration controlled logic.

To be presented by Melanie Berg at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 23-26, 2015.

Xilinx Virtex-5 Results Summary

- A new method for FPGA processor testing has been developed by NEPP (presented at ETW 2014).
- The following are a few of the techniques that were implemented for this test campaign.
  - Fault visibility is increased by extracting internal embedded-PC (DUT) signals and feeding them to the LCDT.
  - The LCDT places watchdog signals on these new observable points.
  - Watchdog failures are noted, time-stamped, and stored to the host PC.
  - The embedded-PC (DUT) signals are also sent to a logic analyzer for real-time observation during irradiation.
  - Cache tests were performed by running full tests internally to cache. All cache-misses can be monitored by external memory accesses.
- Take away: new method has proven to increase visibility of faults:
  - SEU cross sections become more accurate.
  - Component failure analysis is enhanced.

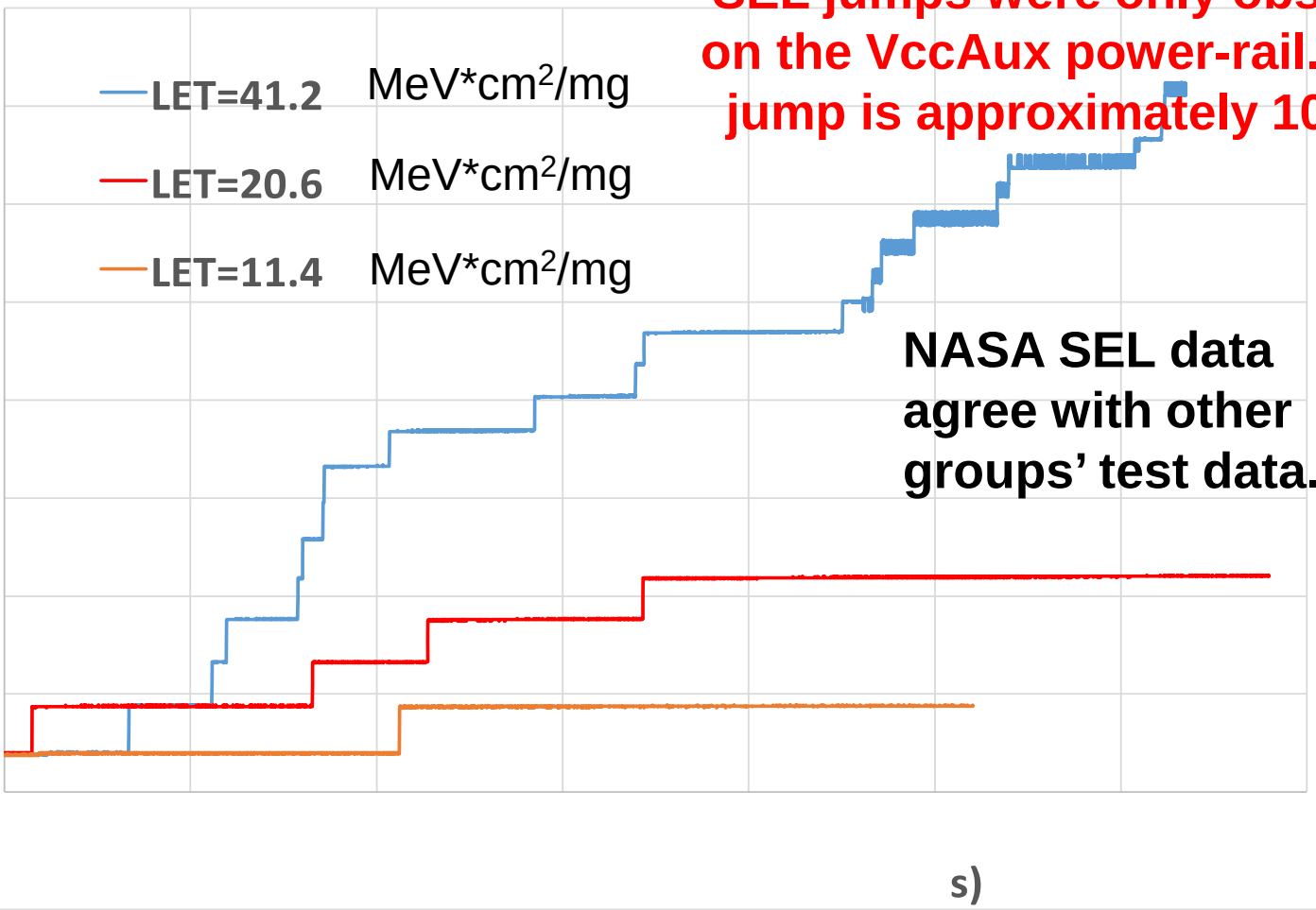
Xilinx Kintex-7 (XC7K325T-1FBG900)
SEL Testing
high-k metal gate (HKMG)
(TSMC 28nm HPL process)

Xilinx Kintex-7 SEL Investigation

- This is an independent study to determine the SEL susceptibility of the Commercial Xilinx Kintex-7 (K7) device.
- Prior SEL testing has been performed by other groups. They have reported observing SEL in the Xilinx 7-series devices.
  - Lee, D.S.; Wirthlin, M.; Swift, G.; Le, A.C., "Single-Event Characterization of the 28 nm Xilinx Kintex-7 Field-Programmable Gate Array under Heavy Ion Irradiation," *Radiation Effects Data Workshop (REDW), 2014 IEEE* , vol., no., pp.1,5, 14-18 July 2014
- NEPP decided to perform follow-up tests for validation.
  - NEPP test procedure was slightly different:
    - Real-time configuration memory scrubbing during irradiation.
    - Analog circuitry monitoring.
    - Custom DUT board was designed to connect with the NEPP LCDT.
    - Temperature variation.
- **Note: SEL is determined by an increase of DUT current that can only be lowered by reducing the DUT power below threshold.**

Sample Kintex-7 SEL Data At Room Temperature

Graph courtesy of David Vail (Harris)

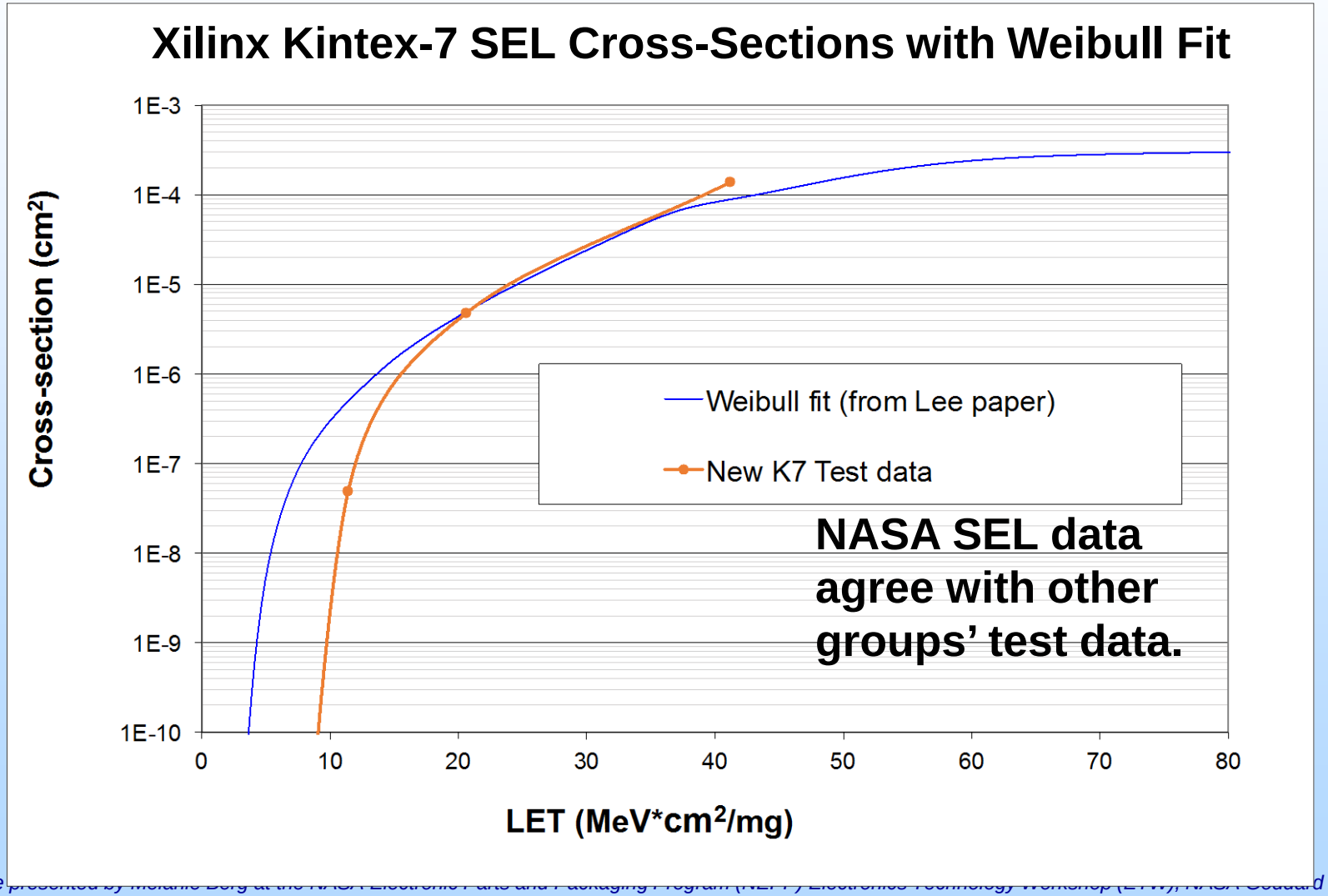


SEL jumps were only observed on the VccAux power-rail. Each jump is approximately 100ms.

NASA SEL data agree with other groups' test data.

Kintex-7 SEL Cross-Section At Room Temperature

Analysis Performed by David Vail (Harris)



Summary of Kintex-7 during SEU-Radiation Testing

- **SEL results concur with other groups:**
  - **With real-time scrubbing.**
  - **However, on-set SEL was observed at a lower LET by NASA/GSFC (11.6MeV*cm^2/mg versus 19MeV*cm^2/mg).**
  - **Had trouble implementing high temperature accelerated radiation testing (power supply issue).**
- **The full Kintex-7 dataset is currently being analyzed and will be available by August 2015.**

SRAM-based FPGA Mitigation Study using Xilinx Kintex-7 (XC7K325T-1FBG900)

(Triple Modular Redundancy (TMR) and Scrubbing)

Mitigation Study Overview

- This is an independent study to determine the effectiveness of various triple modular redundancy (TMR) schemes implemented in SRAM-based FPGA devices.
- TMR schemes are defined by what portion of the circuit is triplicated and where the voters are placed.
  - The strongest TMR implementation will triplicate all data-paths and contain separate voters for each data-path.
  - However, this can be costly: area, power, and complexity.
  - A trade is performed to determine the TMR scheme that requires the least amount of effort and circuitry that will meet project requirements.
- Presentation scope:
  - Block TMR (BTMR), Local TMR (LTMR), Distributed TMR (DTMR), Mixed TMR (PTMR).

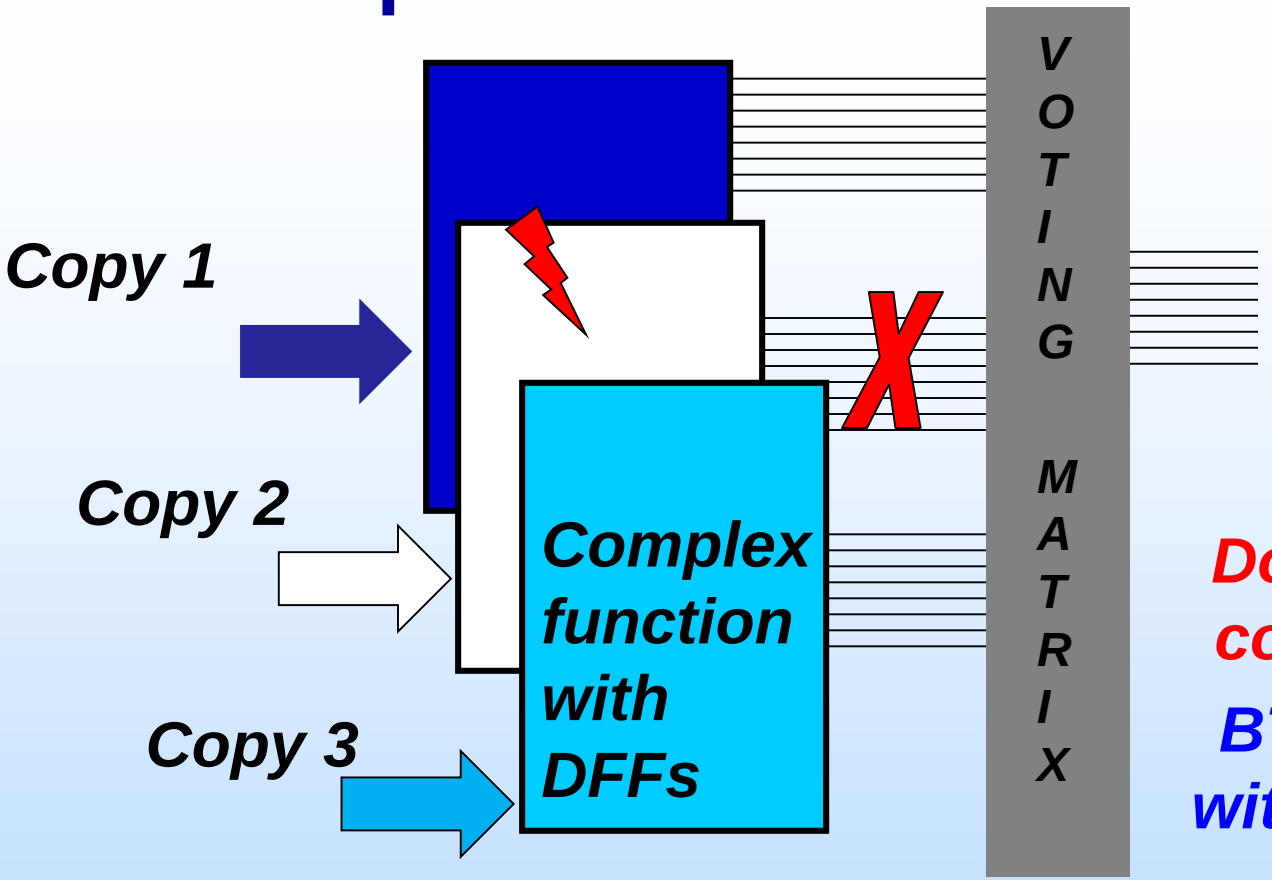
TMR Descriptions

DFF: Edge triggered flip-flop; *CL: Combinatorial Logic*

TMR Nomenclature	Description	TMR Acronym
Block TMR	Entire design is triplicated. Voters are placed at the outputs.	BTMR
Local TMR	Only the DFFs are triplicated. Voters are placed after the DFFs.	LTMR
Distributed TMR	DFFs and CL-data-paths are triplicated. Similar to a design being triplicated but voters are placed after the DFFs.	DTMR
Global TMR	DFFs, CL-data-paths and global routes are triplicated. Voters are placed after the DFFs.	GTMR or XTMR

Note: It is suggested to separate (partition) TMR domains in SRAM based designs so that there are no overlapped shared resources. Shared resources become single points of failure.

Block Triple Modular Redundancy: BTMR



Voting is only at outputs of complex blocks. Can Only Mask Errors

Does not elongate correct operation!

BTMR= downtime with masked failure

- **If one module is expected to fail within time t, then the system is expected to fail within time t.**
- **When one fails, another is expected to fail soon.**
- **Affects availability, upon one module failing, system should stop and flush the error.**

What Should be Done If MTTF or Availability Needs to be Increased?

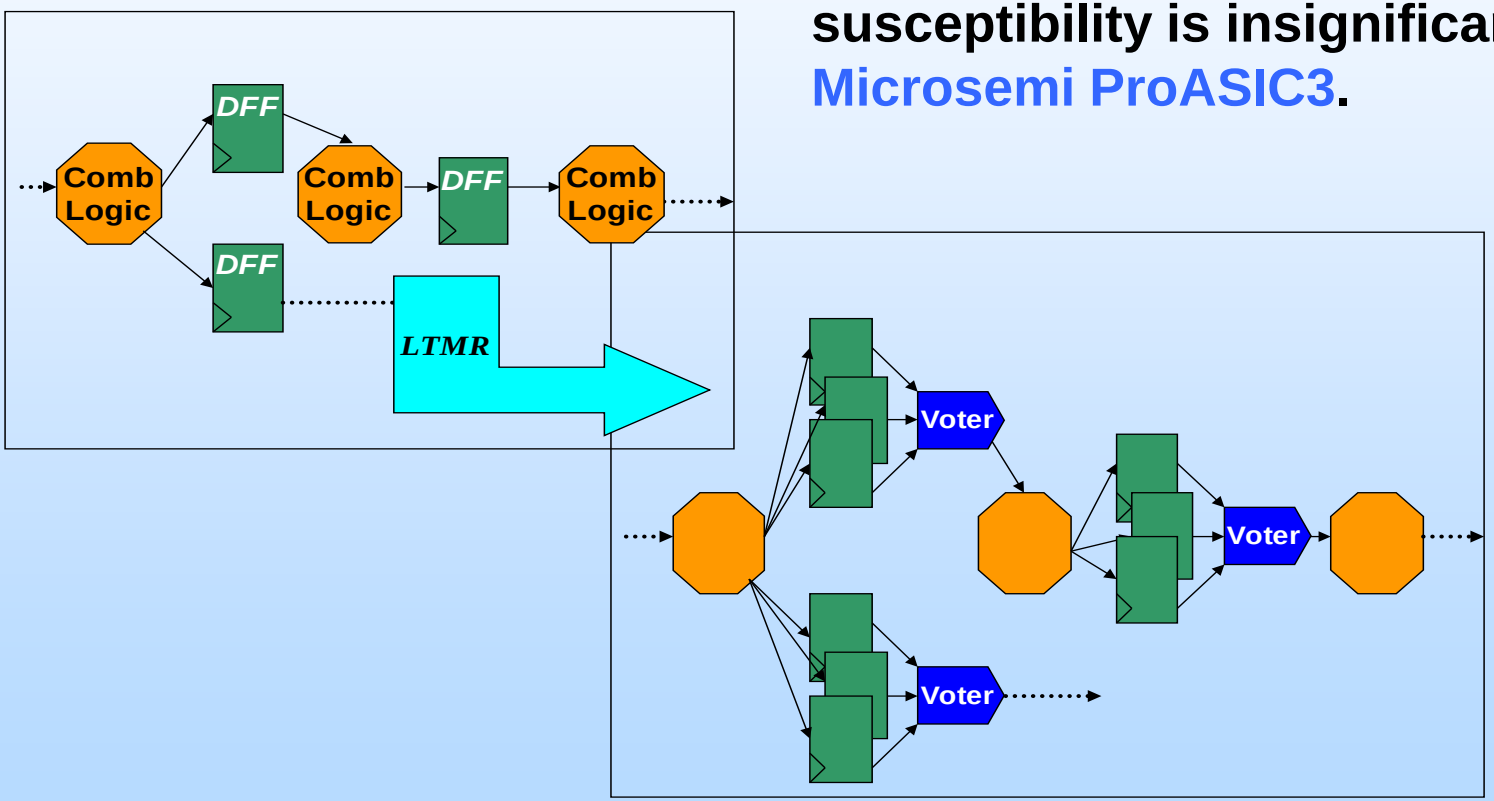
- If the blocks within the BTMR have relatively high upset rates with respect to the required operational window, then stronger mitigation must be implemented.
- Bring the voting/correcting inside of the modules… bring the voting to the module DFFs.

The following slides illustrate the various forms of TMR that include voter insertion in the data-path.

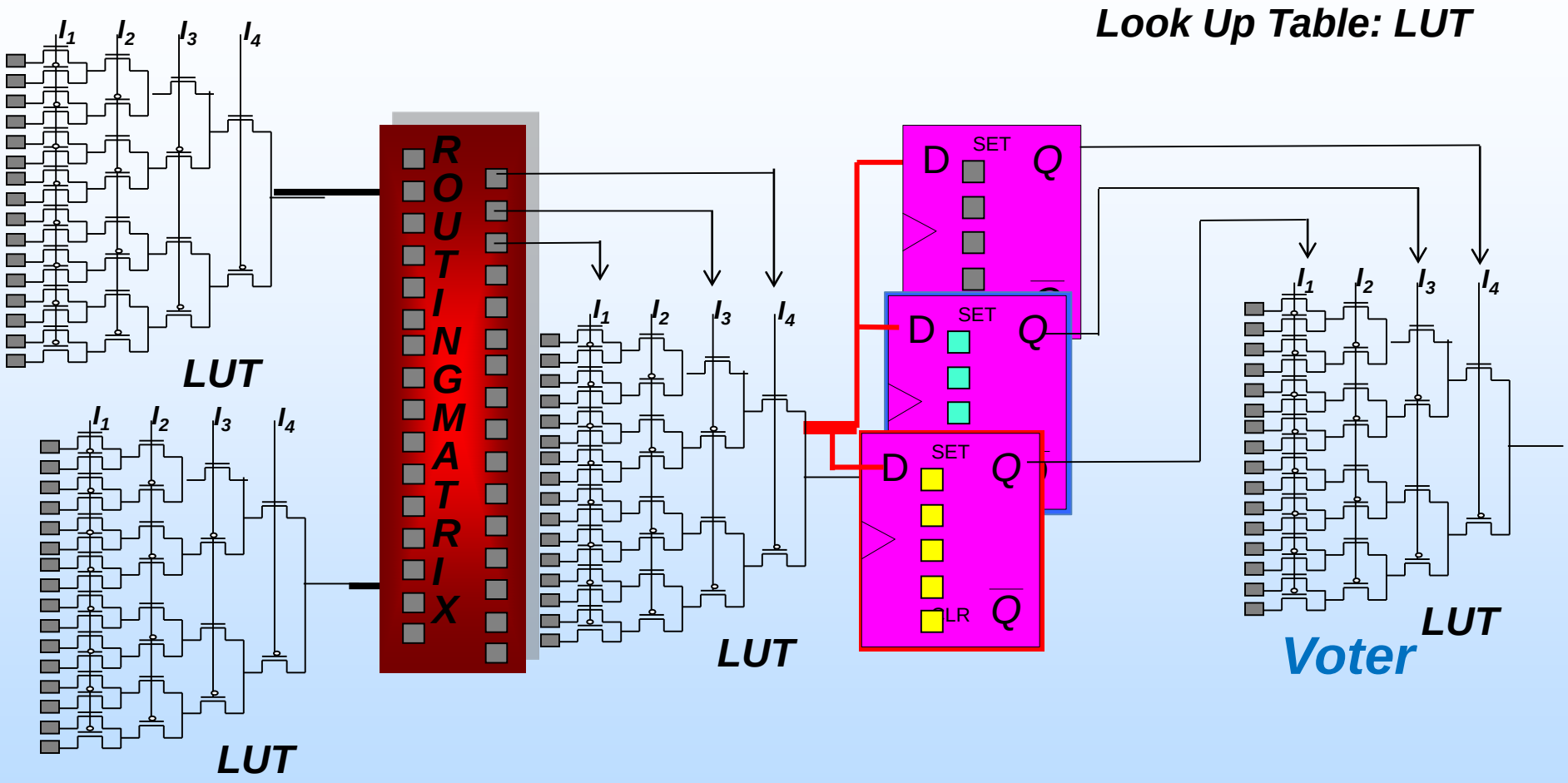
TMR Nomenclature	Description *DFF: Edge triggered flip-flop; CL: Combinatorial Logic*	TMR Acronym
Local TMR	DFFs are triplicated	LTMR
Distributed TMR	DFFs and CL-data-paths are triplicated	DTMR
Global TMR	DFFs, CL-data-paths and global routes are triplicated	GTMR or XTMR

Local Triple Modular Redundancy (LTMR)

- Only DFFs are triplicated. Data-paths are kept singular.
- LTMR masks upsets from DFFs and corrects DFF upsets if feedback is used.
- Good for devices where DFFs are most susceptible and configuration and CL susceptibility is insignificant; e.g., Microsemi ProASIC3.



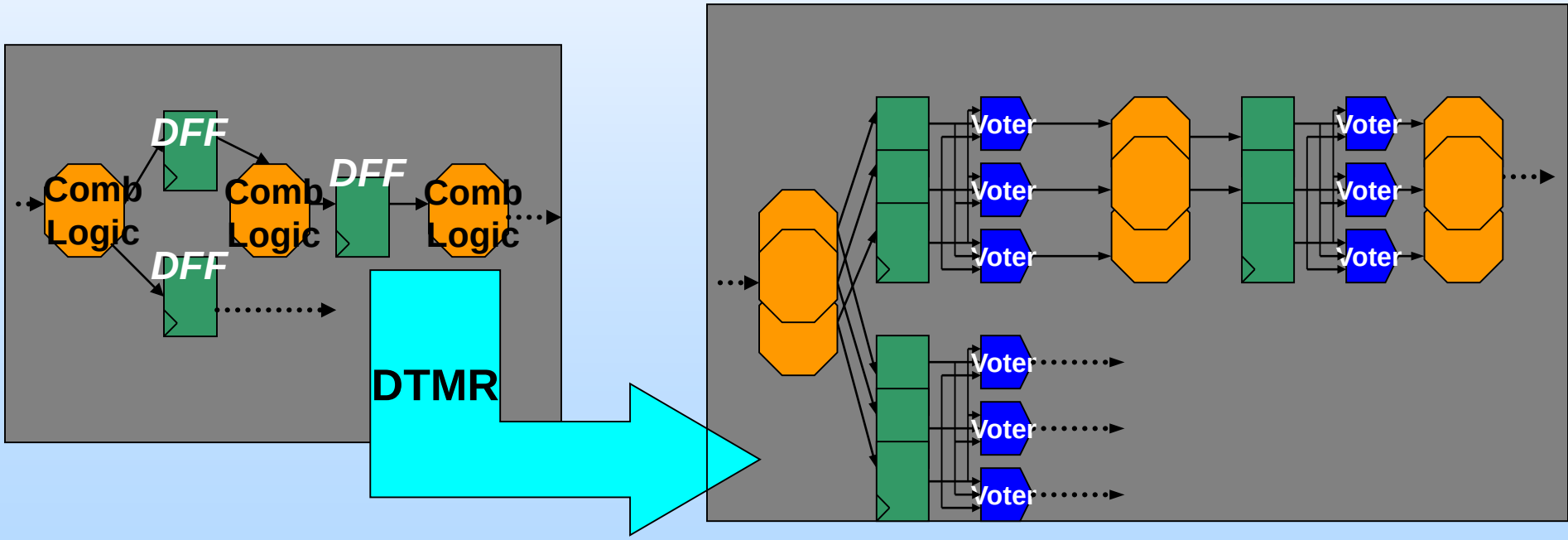
LTMR Should Not Be Used in An SRAM Based FPGA



Too many other configuration bits + logic that can be corrupted by an SEU. Mitigation needs to be stronger than only protecting DFFs.

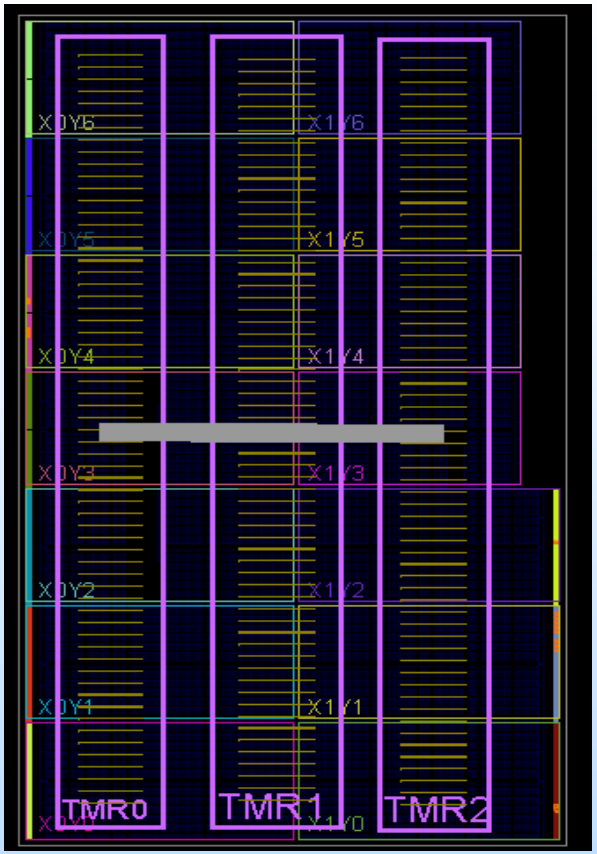
Distributed Triple Modular Redundancy (DTMR)

- Triple all data-paths and add voters after DFFs.
- DTMR masks upsets from configuration + DFFs + CL and corrects captured upsets if feedback is used.
- Good for devices where configuration or DFFs + CL are more susceptible than project requirements; e.g., Xilinx and Altera commercial FPGAs.



When Using TMR in an SRAM Based FPGA, Partitions Should Be Used

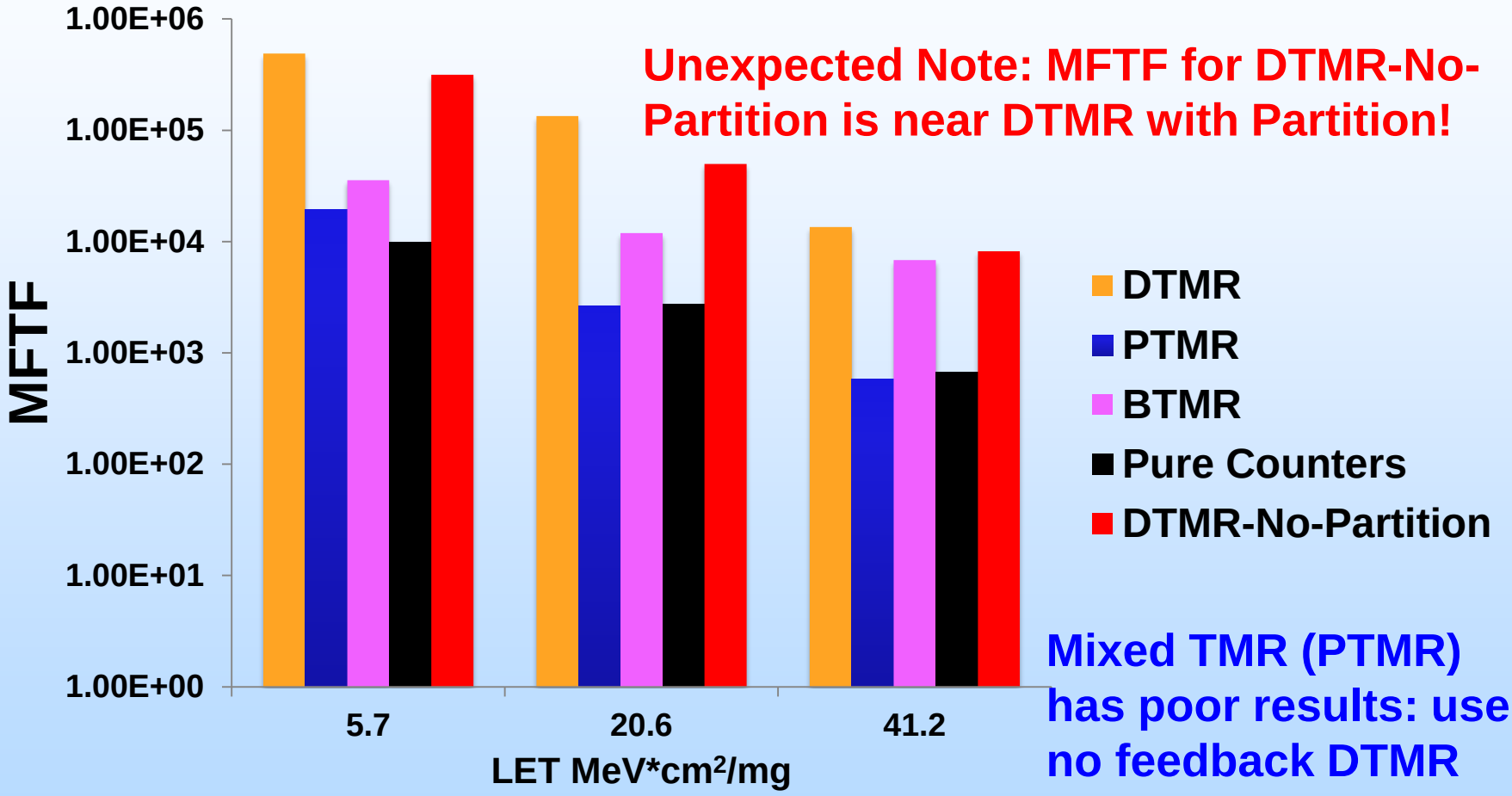
- SRAM based FPGAs use a significant number of shared resources; e.g., routing matrices.
- A resource that is shared across separate TMR domains can break the TMR scheme if hit by an SEU.
- Solution is to partition the TMR domains such that they do not share resources.
- Difficult:
  - Significantly increases area requirements,
  - Significantly reduces performance, and
  - It's getting worse with new generations of devices.



Name TMR domains with unique identifier for easier floor-planning.

Results: Mitigation SEU Data

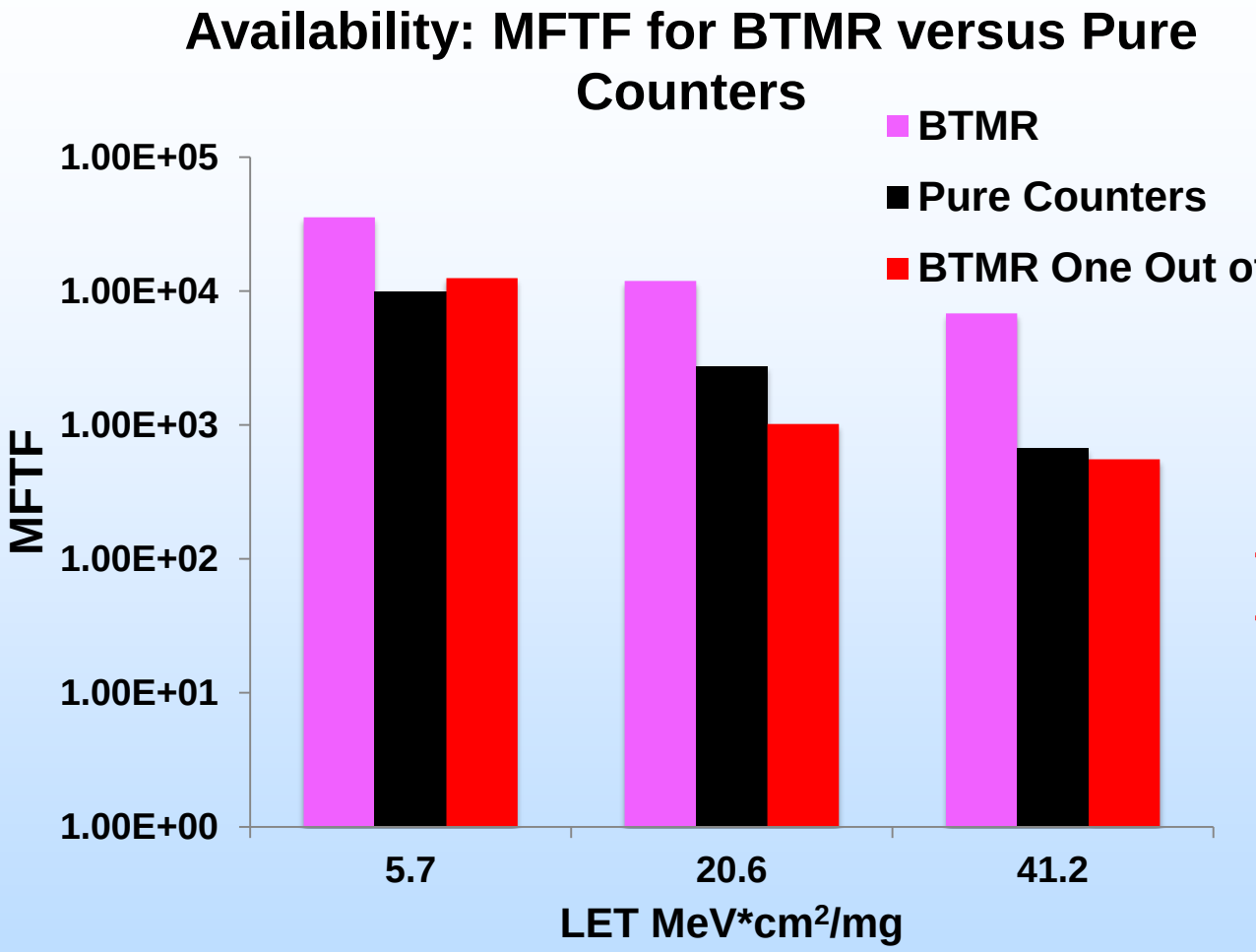
Mean Fluence to Failure (MFTF) for Various Mitigation Strategies



Unexpected Note: MFTF for DTMR-No-Partition is near DTMR with Partition!

Mixed TMR (PTMR) has poor results: used no feedback DTMR and LTMR in some areas.

Results: Availability in Non-Flushable Designs



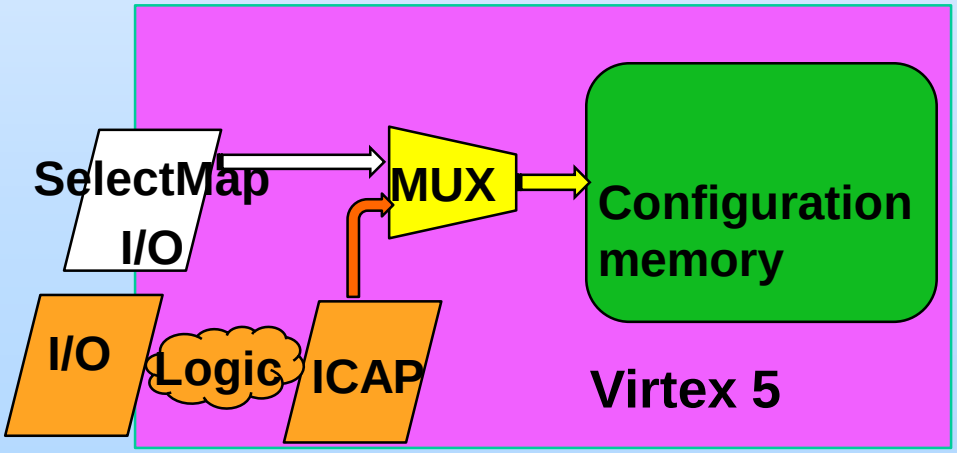
Reliability for BTMR-one-out-of-three can be less than counters with no mitigation!

The Common Strategy Is To Reset The System Upon First Block (component) Error.

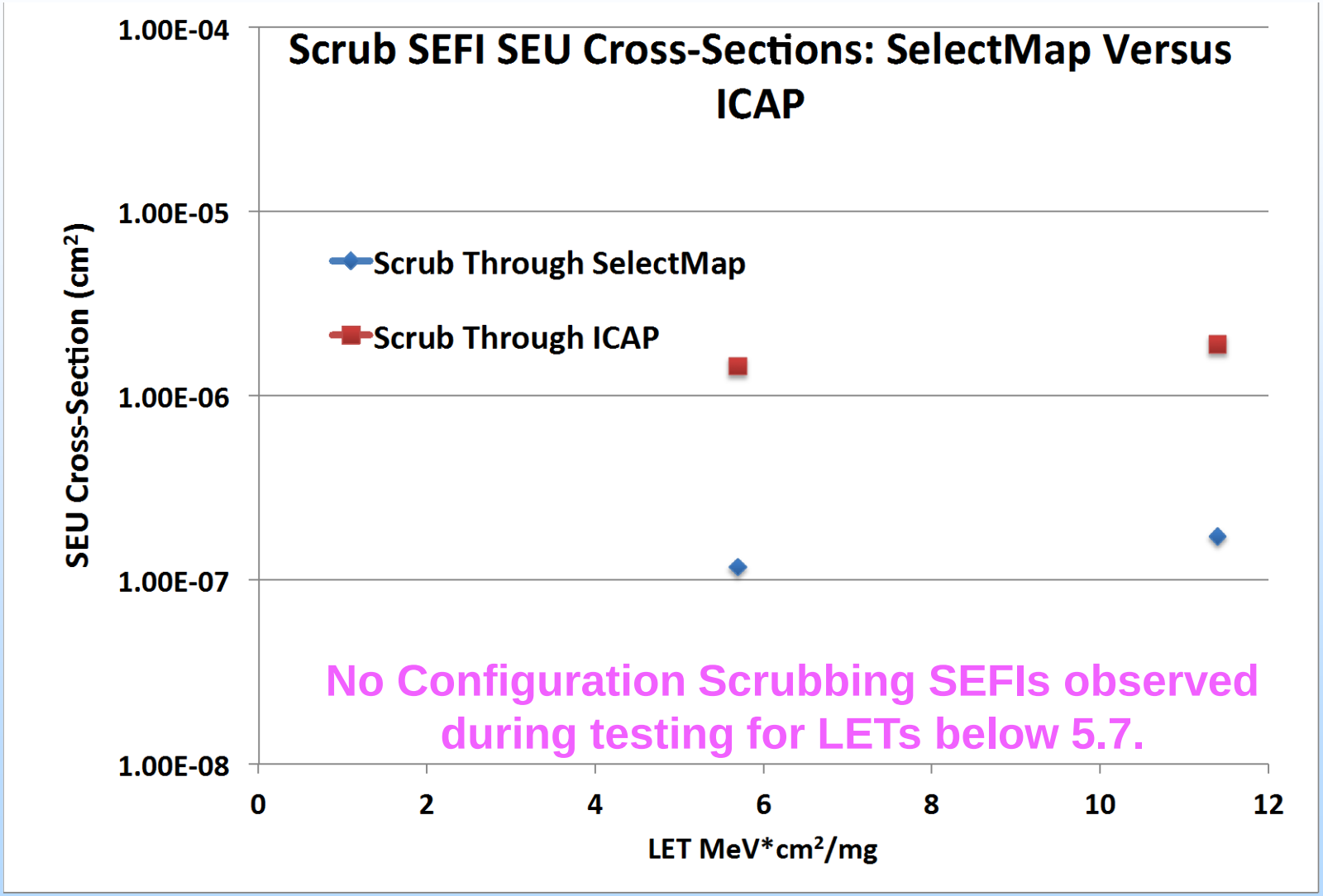
This affects Availability.

Configuration Memory Scrubbing- *Results: SEFIs*

- **Two methods of scrubbing were performed:**
  - **SelectMap (direct from LCDT), and**
  - **Internal configuration access port (ICAP) (Signals sourced from LCDT with feed-through to ICAP).**
- **Both use blind scrubbing – hence can correct any number of configuration memory SEUs.**



Configuration Scrubbing SEFI Cross-Sections:
SelectMap versus ICAP



Summary of Mitigation Application to Kintex-7 during SEU-Radiation Testing

- **Mitigation study proves DTMR is effective for this design implemented in an SRAM-based FPGA.**
  - **However, for flushable designs BTMR might be acceptable.**
  - **LTMR is not acceptable in SRAM-based FPGAs for any design.**
  - **Partitioning may not be necessary.**
- **Internal scrubbing will have a higher SEFI rate and may need further investigation for project usage.**

Plans for FY15 and out:
Microsemi, Xilinx, Altera, and Synopsis.
We Looking for Collaborators

Microsemi RTG4

- New Entry into the Aerospace Market with Space-grade Expectation
  - 65nm
- Custom daughter (DUT) cards are currently being built. Plan to be fabricated and populated by August 2015.
- Prototype evaluation board will be purchased for early design development.
- Phase I tests (date: fall 2015):
  - Shift registers, counters, PLLs, and DSPs.
  - Use of Synopsis tool for mitigation insertion.
- Phase II and Phase III tests (date TBD):
  - High speed serial interfaces (XAUI, PCIe, Spacewire, and Spacefibre), instantiated processor(TBD).
  - Use of Synopsis tool for mitigation insertion.

Altera Stratix-V Radiation Test Development

- New Entry into the Aerospace Market with COTS Expectation
  - 28nm bulk CMOS
- Evaluation boards have been purchased for early design development and early latch-up testing.
  - Custom interface was designed to connect to the LCDT for increased visibility during accelerated radiation testing.
  - Voltage supplies are separated for accurate voltage monitoring.
- Custom daughter (DUT) cards will be built based off of June Testing.
- Phase I tests (date June 2015):
  - Evaluation board latch-up investigation.
- Phase II tests (TBD):
  - Shift registers, counters, PLLs, and DSPs.
  - Use of Synopsis tool for mitigation insertion.
- Phase III tests:(TBD):
  - High speed serial interfaces (TBD), instantiated processor(TBD).
  - Use of Synopsis tool for mitigation insertion.

Xilinx Kintex UltraScale

- New Entry into the Aerospace Market with COTS Expectation
  - 20 nm planar process (TSMC)
- Prototype evaluation board will be purchased for early design development and early latch-up testing.
  - Custom interface will be designed to connect to the LCDT for increased visibility during accelerated radiation testing.
- Phase I tests (date fall 2015 or spring 2016):
  - Evaluation board latch-up investigation.
- Phase II tests (date TBD):
  - Shift registers, counters, PLLs, and DSPs.
  - Use of Synopsis tool for mitigation insertion.
- Phase III tests (TBD):
  - High speed serial interfaces (TBD), embedded processors.

Xilinx Zynq UltraScale+

- New Entry into the Aerospace Market with COTS Expectation
  - 16nm vertical process (TSMC)
- Multi-Processor System on a Chip (MPSoC) family.
- Prototype evaluation board will be purchased for early design development and early latch-up testing.
- Planning to receive parts in spring of 2016.
- Custom daughter (DUT) cards will be built (date TBD).
- Phase I tests (date TBD):
  - Evaluation board latch-up investigation.
- Phase II tests (date TBD):
  - Shift registers, counters, PLLs, and DSPs.
  - Use of Synopsis tool for mitigation insertion.
- Phase III tests (TBD):
  - High speed serial interfaces (TBD), embedded processors.

Conclusions

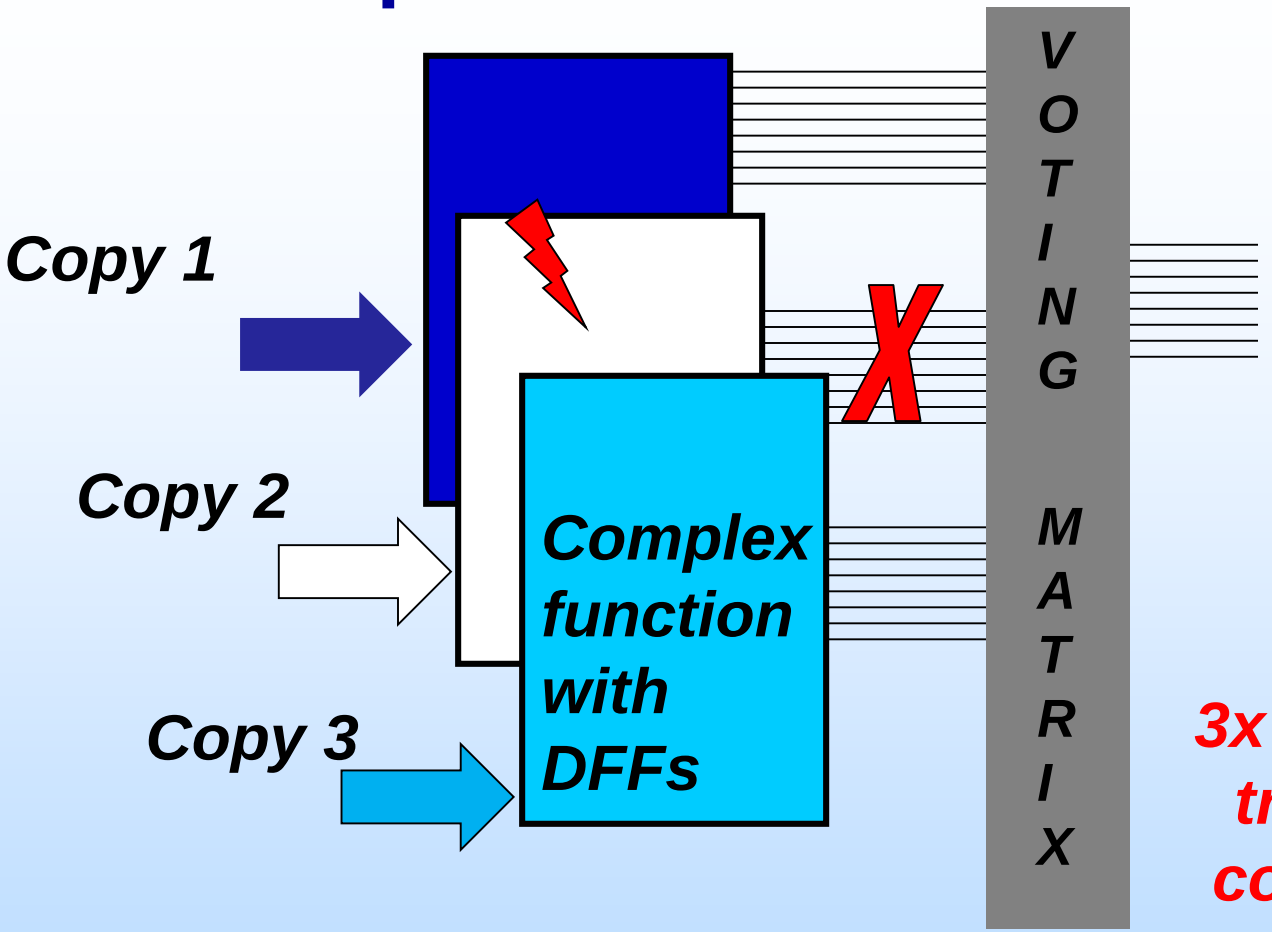
- **NEPP has provided and will continue to investigate:**
  - **New accelerated-radiation test methodologies for FPGA devices and embedded hard-IP (e.g., processors).**
  - **Mitigation strategies specific to FPGA types and how to measure their efficacy for meeting project requirements.**
- **NEPP continues independent investigation of various FPGA devices:**
  - **Destructive mechanisms and SEL.**
  - **SEU characterization.**
  - **Total Ionizing Dose (TID) characterization.**

Acknowledgements

- **Supporters:**
  - **Defense Threat Reduction Agency (DTRA)**
  - **NASA Electronics Parts and Packaging (NEPP) Program**
- **Current Collaborators:**
  - **Xilinx,**
  - **Microsemi,**
  - **Altera,**
  - **Synopsis,**
  - **Harris,**
  - **Honeywell,**
  - **Aerospace Corporation,**
  - **NASA Space Launch System (SLS) mission, and**
  - **NASA Transiting Exoplanet Survey Satellite (TESS) mission.**

BACKUP CHARTS

Block Triple Modular Redundancy: BTMR



Voting is only at outputs of complex blocks. Can Only Mask Errors

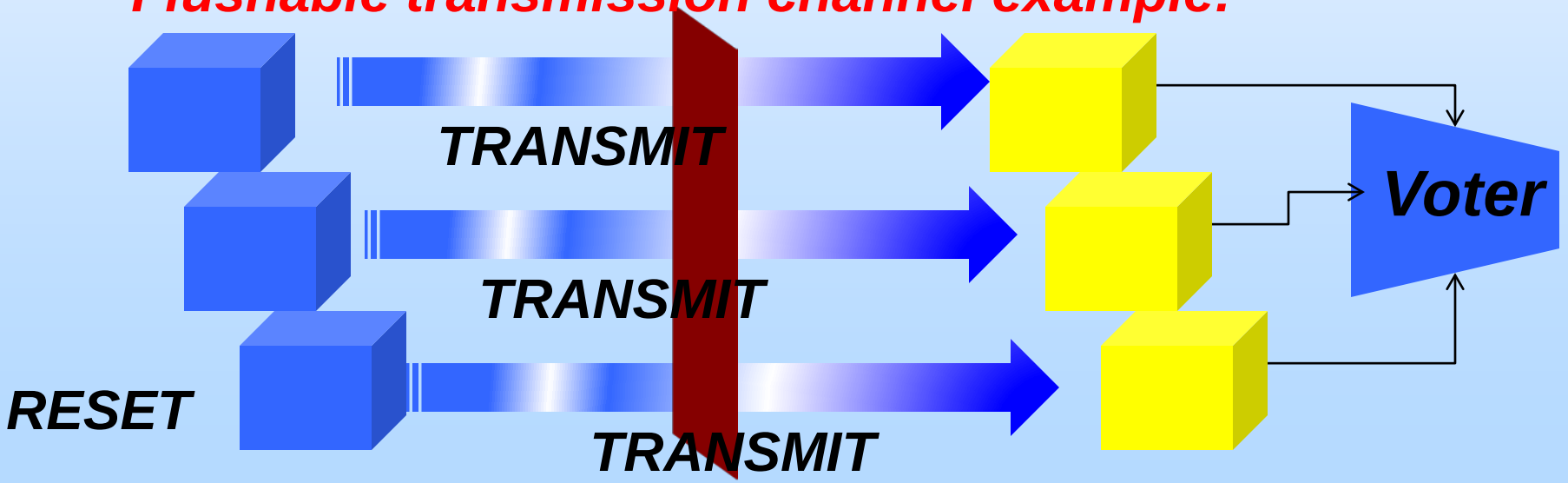
3x the error rate with triplication and no correction/flushing.

- **Need Feedback to DFFS in order to Correct.**
- **Cannot apply internal correction from voted outputs.**
- **If blocks are not regularly flushed (e.g. reset), Errors can accumulate – may not be an effective technique.**

When BTMR Works: Examples of Flushable BTMR Designs

- Shift Registers,
- Finite impulse response (FIRs),
- Transmission channels: It is typical for transmission channels to send and reset after every sent packet,
- Lock-Step microprocessors that have relaxed requirements such that the microprocessors can be reset (or power-cycled) every so-often.

Flushable transmission channel example:

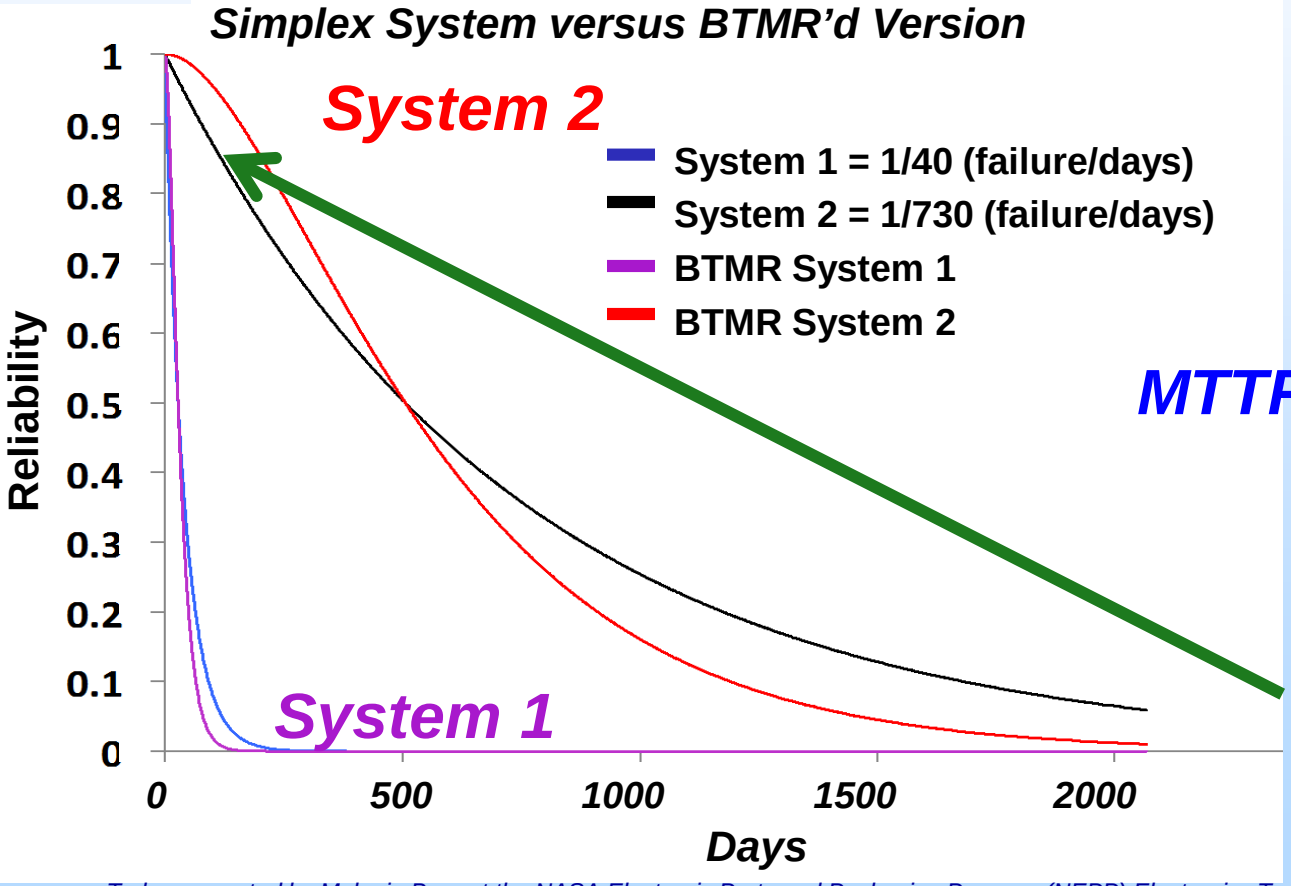


If The System Is Not Flushable, Then BTMR May Not Provide The Expected Level of Mitigation

- With a BTMR scheme, there is no correction, just masking.
  - Voters have no feedback.
  - Voters need to reach DFFs in order to perform correction.
- BTMR can work well as a mitigation scheme if the expected MTTF >> expected (or required) window of correct operation.
- But… If the expected time to failure for one block is less than the required full-liveliness window, then BTMR doesn't buy you anything.
- If not thought out well, BTMR can actually be a detriment – complexity, power, and area, and false sense of performance.

Explanation of BTMR Strength and Weakness using Classical Reliability Models

Relibility for 1 block (R_{block})	Relibility for BTMR (R_{BTMR})	Mean Time to Failure for 1 block ($MTTF_{block}$)	Mean Time to Failure BTMR ($MTTF_{BTMR}$)
$e^{-\lambda t}$	$3\,e^{-2\lambda t}-2\,e^{-3\lambda t}$	$1/\lambda$	$(5/6\,\lambda)= 0.833/\lambda$



$$\lambda = \frac{Failures}{Time}$$

SEU Data

Overall:

$MTTF_{BTMR} < MTTF_{Block}$

Operating in this time interval will provide a slight increase in reliability.

However, it will provide a relatively hard design.

What Should be Done If Availability Needs to be Increased?

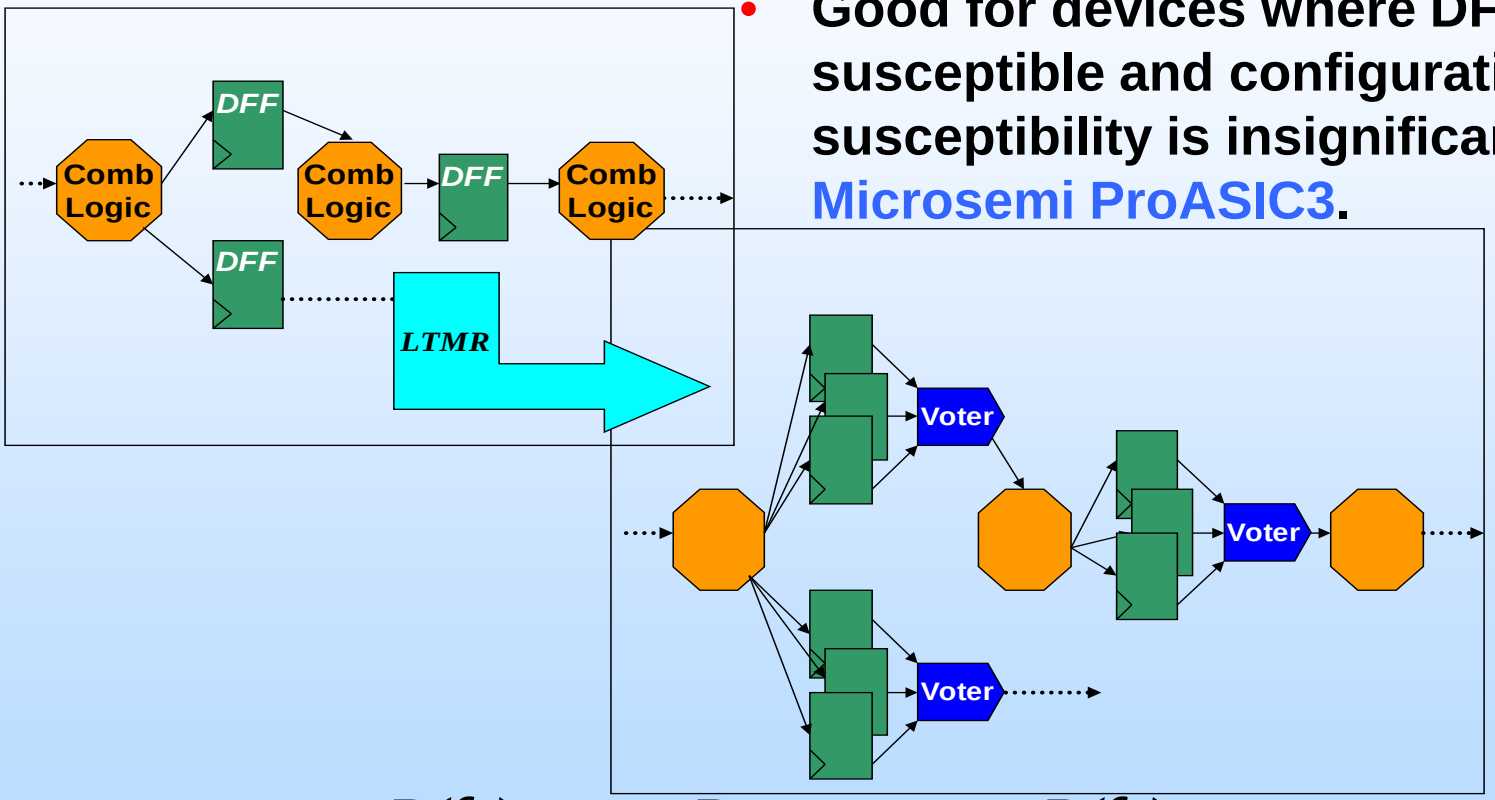
- If the blocks within the BTMR have a relatively high upset rate with respect to the required operational window, then stronger mitigation must be implemented.
- Bring the voting/correcting inside of the modules… bring the voting to the module DFFs.

The following slides illustrate the various forms of TMR that include voter insertion in the data-path.

TMR Nomenclature	Description *DFF: Edge triggered flip-flop; CL: Combinatorial Logic*	TMR Acronym
Local TMR	DFFs are triplicated	LTMR
Distributed TMR	DFFs and CL-data-paths are triplicated	DTMR
Global TMR	DFFs, CL-data-paths and global routes are triplicated	GTMR or XTMR

Local Triple Modular Redundancy (LTMR)

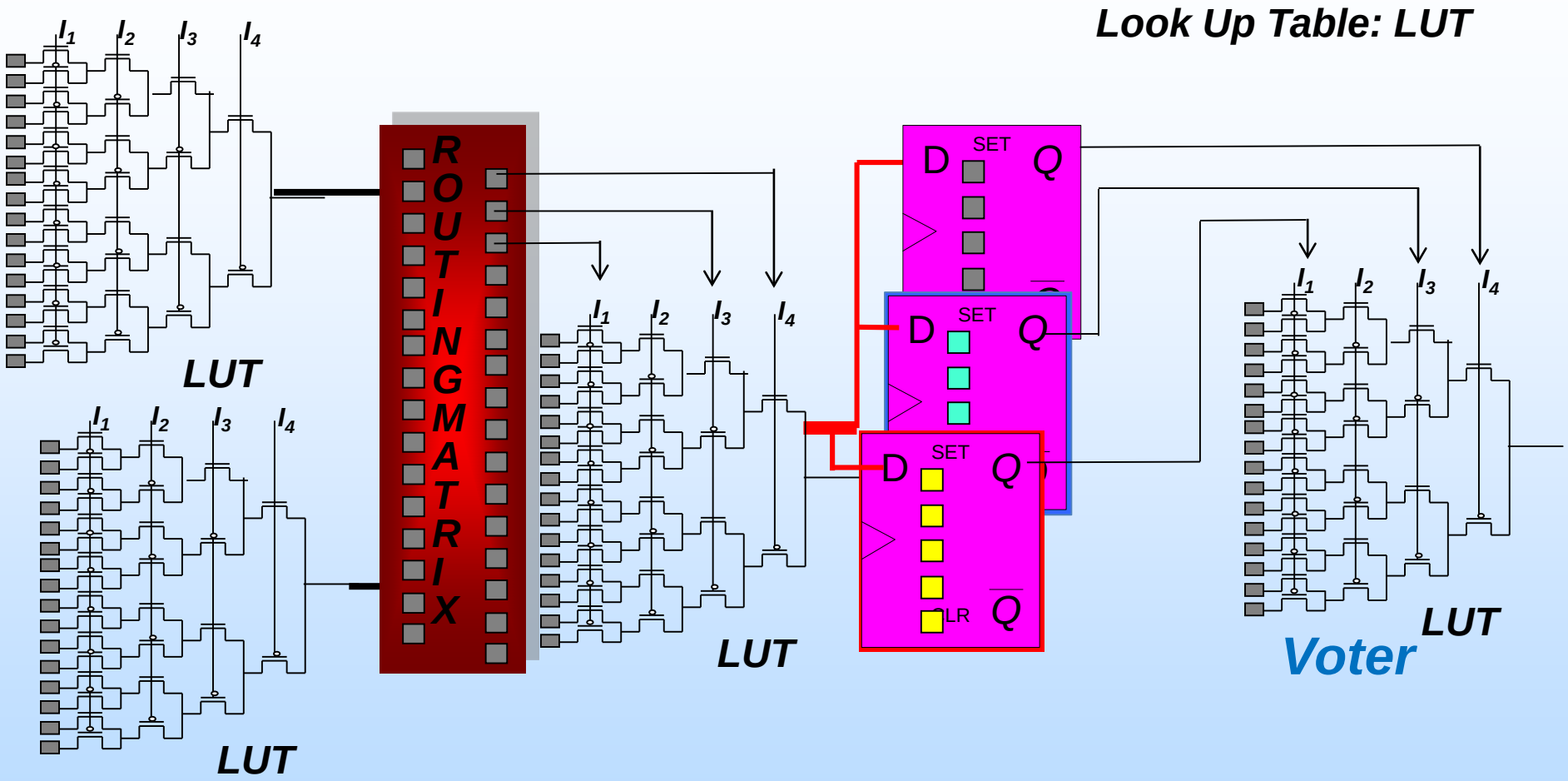
- Only DFFs are triplicated. Data-paths are kept singular.
- LTMR masks upsets from DFFs and corrects DFF upsets if feedback is used.
- Good for devices where DFFs are most susceptible and configuration and CL susceptibility is insignificant; e.g., Microsemi ProASIC3.



$$P(fs)_{error} \propto P_{configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

$$P(fs)_{DFFSEU \rightarrow SEU} + P(fs)_{SET \rightarrow SEU} \rightarrow 0$$

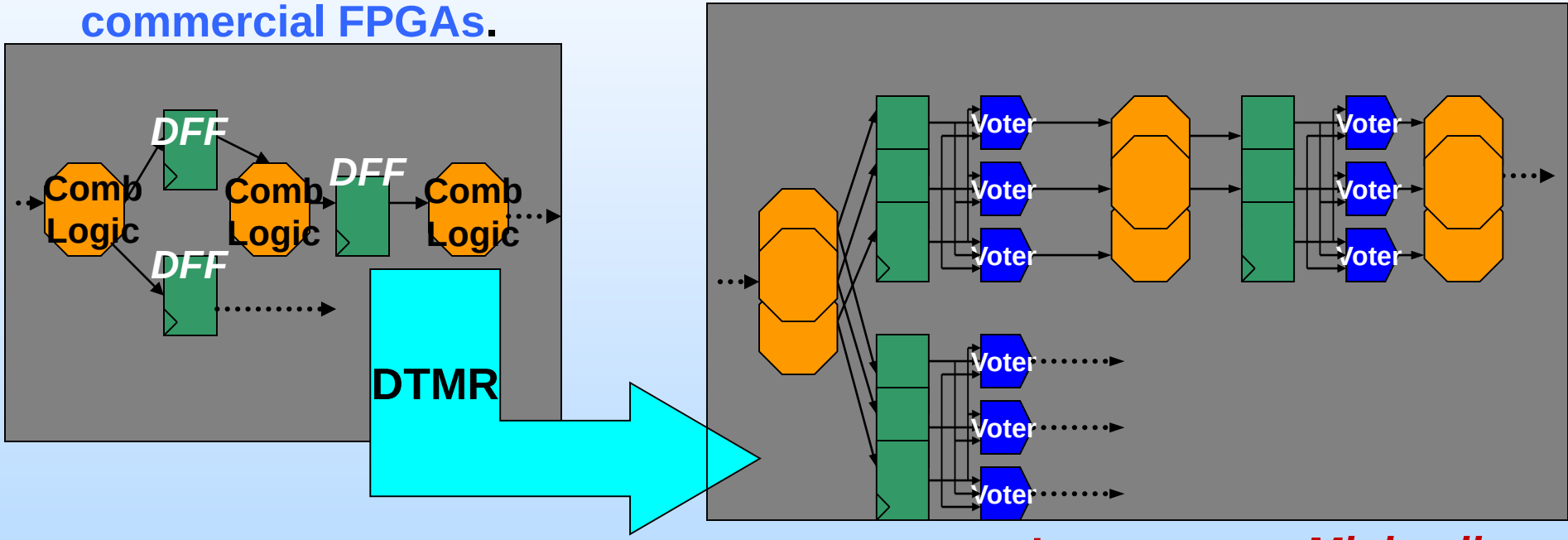
LTMR Should Not Be Used in An SRAM Based FPGA



Too many other configuration bits + logic that can be corrupted by an SEU. Mitigation needs to be stronger than only protecting DFFs.

Distributed Triple Modular Redundancy (DTMR)

- Triple all data-paths and add voters after DFFs.
- DTMR masks upsets from configuration + DFFs + CL and corrects captured upsets if feedback is used.
- Good for devices where configuration or DFFs + CL are more susceptible than project requirements; e.g., Xilinx and Altera commercial FPGAs.



$$P(f_s)_{error} \propto P_{configuration} + P(f_s)_{functionalLogic} + P_{SEFI}$$

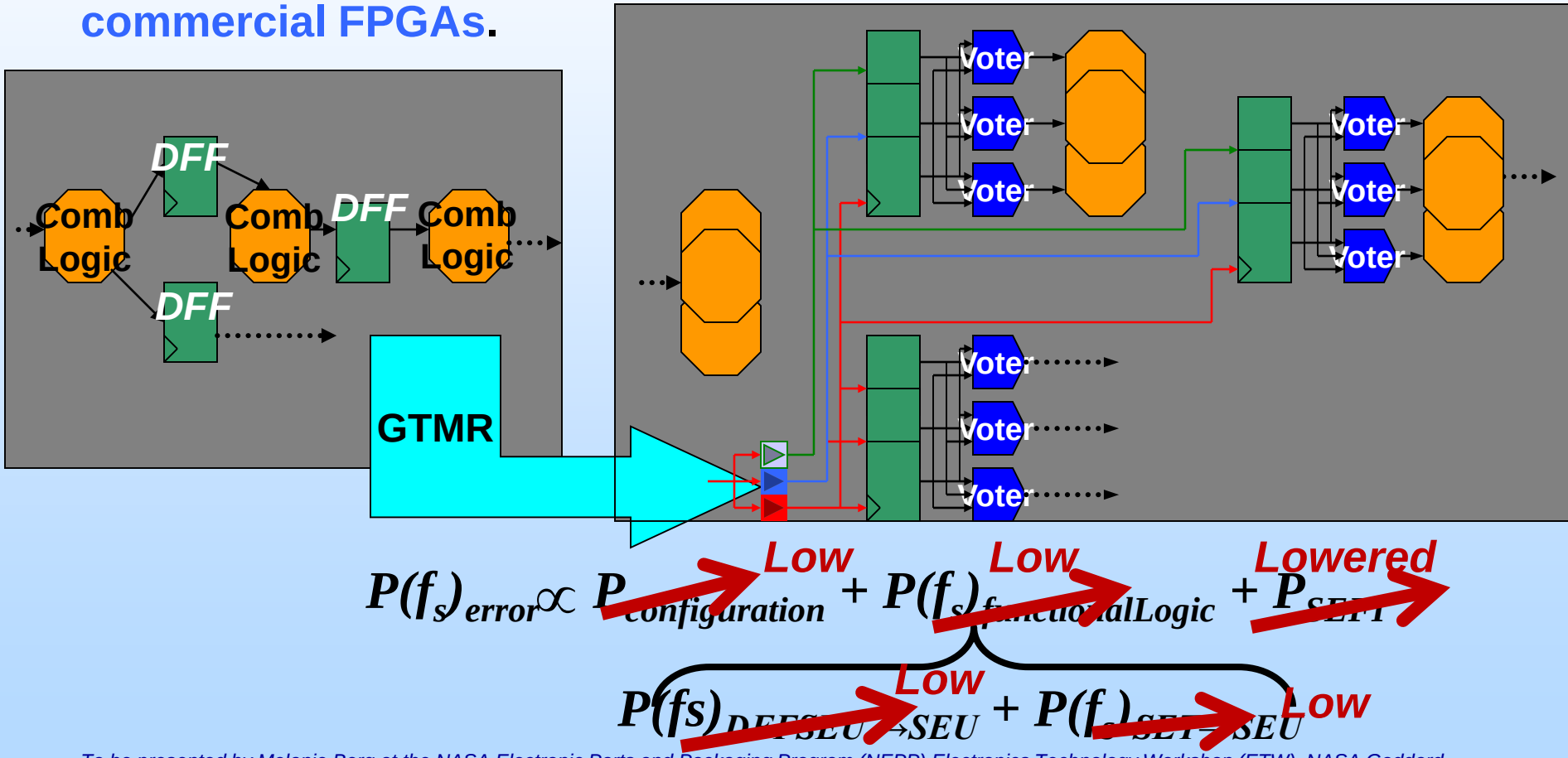
Low — Minimally Lowered

$$P(fs)_{DFFSEU \rightarrow SEU} + P(f_s)_{SET \rightarrow SEU}$$

0 — Low

Global Triple Modular Redundancy (GTMR)

- Triple all clocks, data-paths and add voters after DFFs.
- GTMR has the same level of protection as DTMR; however, it also protects clock domains.
- Good for devices where configuration or DFFs + CL are more susceptible than project requirements; e.g., Xilinx and Altera commercial FPGAs.

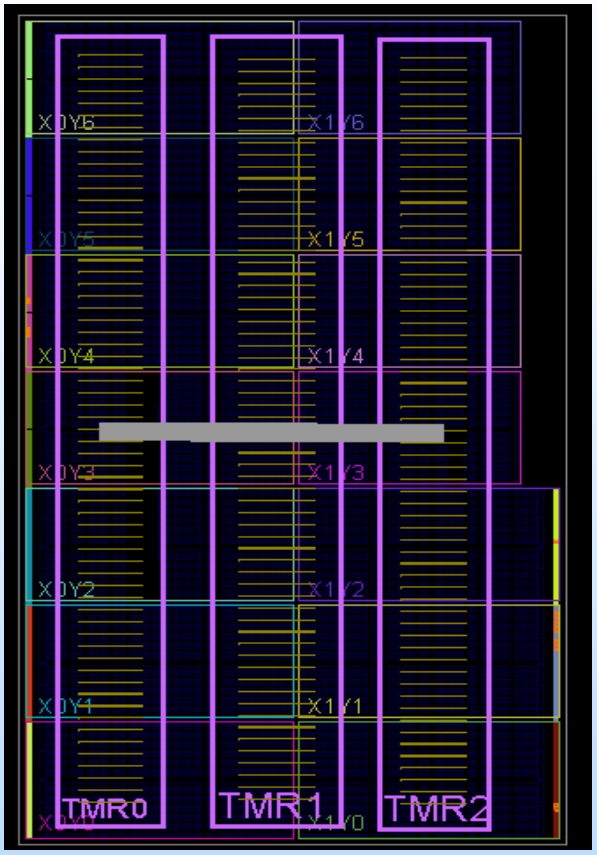


Theoretically, GTMR Is The Strongest Mitigation Strategy… BUT…

- Triplicating a design and its global routes takes up a lot of power and area.
- Generally performed after synthesis by a tool– not part of RTL.
- Skew between clock domains must be minimized such that it is less than the feedback of a voter to its associated DFF:
  - Does the FPGA contain enough low skew clock trees? (each clock + its synchronized reset)x3.
  - Limit skew of clocks coming into the FPGA.
  - Limit skew of clocks from their input pin to their clock tree.
- Difficult to verify.

When Using TMR in an SRAM Based FPGA, Partitions Should Be Used

- SRAM based FPGAs use a significant number of shared resources; e.g., routing matrices.
- A resource that is shared across separate TMR domains can break the TMR scheme if hit by an SEU.
- Solution is to partition the TMR domains such that they do not share resources.
- Difficult:
  - Significantly increases area requirements,
  - Significantly reduces performance, and
  - It's getting worse with new generations of devices.



Name TMR domains with unique identifier for easier floor-planning.